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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,593	11/21/2003	Peng-Cheng Shi	WB88116	3275

7590 11/21/2005

JIANQ CHYUN
INTELLECTUAL PROPERTY OFFICE
7F-1, NO. 100, ROOSEVELT RD.
SEC. 2
TAIPEI 100,
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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,593	SHI, PENG-CHENG	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-5 and 7-16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5, 7-9, 11-14 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Howland (6894519).

Regarding claim 1, Howland disclose [Fig. 4] a method for detecting electrostatic charges (within region 44, area 22 and layer 45) on a wafer (wafer 12) surface (top surface 24), comprising the steps of: (a) disposing a capacitor plate (dielectric layer 36) above a wafer surface (24) on which electrostatic charges are to be scanned, wherein the capacitor plate (36) comprises [see Fig. 5] a plurality of capacitor sub-plates (20) electrically insulated from each other [via insulating layer 54]; (b) using a movable probe (probe 14) to measure voltages at various locations at the capacitor plate (36); (c) collecting the measured voltage distribution [via means for measuring response 30], and (d) examining the collected voltage distribution [via means for

measuring response 30] to identify areas on the wafer surface (24) correspondingly to high electrostatic charge density.

Regarding claim 2, Howland discloses the wafer (12) contains a dielectric layer (dielectric layer 36) at its outmost surface.

Regarding claim 3, Howland discloses the dielectric layer (36) is an oxide layer.

Regarding claim 5, Howland discloses the capacitor plate (36) is structured such that it can be moved both vertically and horizontally [via chuck 28] above the wafer surface (24).

Regarding claim 7, Howland discloses [se Fig. 4] a method for detecting electrostatic charges (within region 44, area 22 and layer 45) on a wafer (wafer 12) surface (top surface 24), comprising the steps of: (a) disposing a capacitor plate (dielectric layer 36) above a wafer surface (24) on which electrostatic charges are to be scanned wherein the capacitor plate (36) comprises [see Fig. 5] a plurality of capacitor sub-plates (20) electrically insulated from each other [via insulating layer 54]; (b) attaching a probe (probe 14) on the capacitor plate (36); (c) moving [via chuck 28] the capacitor plate (36) horizontally above the wafer surface (24) so as to allow the probe (14) to measure voltages at various locations above the wafer surface(24); (d) collecting the measured voltage distribution [via means for measuring response 30], and (e) examining the collected voltage distribution [via means for measuring response 30] to identify areas on the wafer surface (24) correspondingly to high electrostatic charge density.

Regarding claim 8, Howland discloses the wafer (12) contains a dielectric layer (dielectric layer 36) at its outmost surface.

Regarding claim 9, Howland discloses the dielectric layer (36) is an oxide layer.

Regarding claim 11, Howland discloses the capacitor plate (36) is structured such that it can be moved both vertically and horizontally [via chuck 28] above the wafer surface (24).

Regarding claim 12, Howland discloses [see Fig. 4] an apparatus method for detecting electrostatic charges (within region 44, area 22 and layer 45) on a wafer (wafer 12) surface (top surface 24), comprising the steps of: (a) movable [via chuck 28] capacitor plate (dielectric layer 36) to be placed above a wafer surface (24) on which electrostatic charges are to be scanned wherein the capacitor plate (36) comprises [see Fig. 5] a plurality of capacitor sub-plates (20) electrically insulated from each other [via insulating layer 54]; (b) a movable probe (probe 14) to measure voltages at various locations at the capacitor plate (36), and (c) a recorder (means for measuring response 30) to collect and record the measured voltage distribution.

Regarding claim 13, Howland discloses the wafer (12) contains a dielectric layer (dielectric layer 36) at its outmost surface.

Regarding claim 14, Howland discloses the dielectric layer (36) is an oxide layer.

Regarding claim 16, Howland discloses the capacitor plate (36) is structured such that it can be moved both vertically and horizontally [via chuck 28] above the wafer surface (24).

Regarding claim 17, Howland discloses the capacitor plate (36) is made of a plurality of capacitor sub-plates (area 22) electrically insulated from each other.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4, 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Howland (6894519) in view of Jolley (5489557).

Regarding claims 4, 10 and 15, Howland discloses [see Fig. 4] an apparatus method for detecting electrostatic charges (within region 44, area 22 and layer 45) on a wafer (wafer 12) surface (top surface 24). However, he does not disclose a cleansing step using water as claimed. Jolley discloses a cleansing step using pure water or de-ionized water to remove particles or other impurities on the wafer surface [see col. 3, line 60- col. 4, line 12]. Further, Jolley teaches that the addition of a cleansing step using water is advantageous because it helps remove particles or other impurities on the wafer surface after testing. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Howland by adding a cleansing step using water as taught by Jolley in order to remove particles or other impurities on the wafer surface after testing.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
November 15, 2005